

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

DEPRAJ S. PUAR

Application No.: Unassigned

Filed: Herewith

For: GRAPHICS CONTROLLER  
INTEGRATED CIRCUIT  
WITHOUT MEMORY INTERFACE

Atty. Docket No.: NEOMP002C2D1

Examiner: Unassigned

Group: Unassigned

Date: March 18, 2004

**INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §§1.56 AND 1.97(c)**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

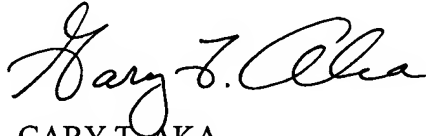
Dear Sir:

The references listed in the attached PTO Form 1449 may be material to examination of the above-identified patent application. Applicants submit the list of these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application. The above-identified application is a divisional application of prior application U.S. Patent Application No. 10/042,952, filed January 7, 2002. This prior application is being relied upon for an earlier filing date under 35 U.S.C. § 120. Because the listed references were either cited by the PTO, or submitted to the PTO in the prior application, under 37 CFR § 1.98(d) Applicants submit that copies need not be provided.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is being filed within three (3) months of the filing date of the above-referenced application. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 50-1652 (Order No. NEOMP002C2D1).

Respectfully submitted,

A handwritten signature in cursive script, appearing to read "Gary T. AKA".

GARY T. AKA  
Reg. No. 29,038

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<b>Form 1449 (Modified)</b>  <b>Information Disclosure Statement By Applicant</b>  (Use Several Sheets if Necessary)	Atty Docket No.	NEOMP002C2D1
	Application No.:	Unassigned
	Inventor	DEEPRAJ S. PUAR et al.
	Group	Unassigned
	Filing Date	Herewith
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### U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-Class	Filing Date
	AA	4,191,956	3/1980	Groothuis	345	201	
	AB	4,228,528	10/1980	Cenker	365	200	
	AC	4,303,986	12/1981	Lans	364	900	
	AD	4,330,849	05/1982	Togei et al.	365	181	
	AF	4,472,792	09/1984	Shimohigashi et al.	365	189	
	AG	4,656,605	04/1987	Clayton	365	52	
	AH	4,691,295	09/1987	Erwin	345	188	
	AI	4,740,782	04/1988	Aoki et al.	345	205	
	AJ	4,812,836	03/1989	Kurakake et al.	345	201	
	AK	4,816,815	03/1989	Yoshiba	345	201	
	AL	4,951,232	08/1990	Hannah	345	189	
	AM	4,956,708	09/1990	Itagaki	348	441	
	AN	5,027,212	06/1991	Marlton et al.	348	512	
	AO	5,031,092	07/1991	Edwards et al.	395	375	
	AP	5,083,047	01/1992	Horie	326	45	
	AQ	5,083,294	01/1992	Okajima	365	200	
	AR	5,144,223	09/1992	Gillingham	323	313	
	AS	5,170,154	12/1992	Mantopoulos	345	27	
	AT	5,198,708	03/1993	Gillingham	326	93	
	AU	5,353,402	10/1994	Lau	395	162	
	AV	5,473,573	12/1995	Rao	365	230.01	
	AW	5,650,955	07/1997	Puar et al.	365	51	
	AX	5,703,806	12/1997	Puar et al.	365	51	
	AY	6,346,946	02/2002	Jeddeloh	345	503	
	AZ	6,424,658	07/2002	Mathur	370	429	

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	Mailing Date	March 18, 2004

**Foreign Patent or Published Foreign Patent Application**

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub- Class	Translation	
							Yes	No
	BA	0 165 441	12/1985	European Pat. Off.				
	BB	0 260 578	03/1988	European Pat. Off.				
	BC	0 334 524	09/1989	European Pat. Off.				
	BD	0 383 080	08/1990	European Pat. Off.				
	BE	0 474 366	03/1992	European Pat. Off.				
	BF	0 492 840	07/1992	European Pat. Off.				
	BG	0 547 892	06/1993	European Pat. Off.				
	BH	3 628 286	02/1988	Germany				
	BI	4-211293	08/1992	Japan				
	BJ	2 217 066	10/1987	United Kingdom				
	BK	2 208 344	03/1989	United Kingdom				

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	Mailing Date	March 18, 2004

**Other Documents**

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	BL	Sato et al. "A Wafer-Scale-Level System Integrated LSI Containing Eleven 4-Mb DRAM's, six 64-kb SRAM's, and an 18K-Gate Array," <i>IEEE J. of Solid-State Circuits</i> (1992) 27:1608-1613.
	BM	Fujita et al., "IMAP: Integrated Memory Array Processor Toward a GIPS Order SIMD Processing LSI," <i>IEICE Trans. Electron.</i> (1993) E76-C:1144-1150.
	BN	IBM Technical Disclosure Bulletin, 35(1A):45-46, June 1992.
	BO	NEC Research and Development, vol. 33, No. 4, Oct. 1992, Tokyo, JP, pp. 585-594, "Integrated Memory Array Processor."
	BP	IEEE Journal of Solid-State Circuits, vol. 25, No. 1, February 1990, N.Y., pp. 30-35, "A 50 MHz 8 Mbit Video Ram with a Column Direction Drive Sense Amplifier."
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.